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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/527,343	03/17/2000	Timothy E. Giorgetta	AMCC4100	3311

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EXAMINER	
WILSON, ROBERT W	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 11/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/527,343	GIORGETTA ET AL.	
	Examiner	Art Unit	
	Robert W Wilson	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19,23-29 and 31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19,23-29 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1.0 The application of Giorgetta et. al. entitled TRANSPOSABLE FRAME STRUCTURE filed on 3/17/2000 and amended on 10/19/04 was examined. **Claims 19, 23-29, & 31** are pending. The examiner discovered a new reference Ikemura (U.S. Patent No.: 5,400,369) which the examiner believes reads on the claimed invention; consequently, the examiner has rewritten this as a non-final rejection.

Claim Rejections - 35 USC § 103

2.0 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3.0 **Claims 19, 23-26, 28, & 29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishimatsu (U.S. Patent No.: 6,018,406) in view of Ikemura (U.S. Patent No.: 5,400,369).

Referring to **Claim 19**, Ishimatsu (U.S. Patent No.: 6,018,406) teaches: A selectable frame synchronization structure transmission repeater (Fig 2 & Fig 3)

A repeater input port to accept a first stream of information including a first arrangement of synchronization bits (600-1, 600-2,...600-m per Fig 3. Please note that it would have been obvious to one of ordinary skill in the art at the time of the invention to integrate the functions of 100 and 200 per Fig 3 into a single unit in order to save space)

Decoder having a first input connected to the repeater input port to receiving the first stream of information (126 per Fig 2. Please note that it would have been obvious to one of ordinary skill in the art at the time of the invention to integrate the functions of 100 and 200 per Fig 3 into a single unit in order to save space)

Ishimatsu does not expressly call for: the decoder reading the first arrangement of synchronization bits to organize the first stream of information into a first frame structure including a data section and a header section, having a plurality of M bits, the decoder having a second input for selecting the first arrangement of synchronization bits to be read by selecting a number of synchronization bits in the range from zero to m bits, selecting the bit position of the synchronization bits in the header section, and selecting the content of each synchronization bit in the header section but teaches SONET decoding per Figs 2 & 3.

Ikemura (U.S. Patent No.: 5,400,369) teaches: the decoder reading the first arrangement of synchronization bits to organize the first stream of information into a first frame structure including a data section and a header section, having a plurality of M bits, the decoder having a second input for selecting the first arrangement of synchronization bits to be read by selecting a number of synchronization bits in the range from zero to m bits, selecting the bit position of the synchronization bits in the header section, and selecting the content of each synchronization bit in the header section (The frame aligner or decoder per Fig 2 is trying to find the A1 byte and A2 byte in the STM-N frame per Fig 1 so that it can determine the frame structure of the STM frame shown in Fig 1. The decoder has a DATA SCANNER per Fig 2 searches for the value of A1 shown in Figure 1 by selecting bits 1 to 8, 2 to 9 and so on or selecting the first arrangement of synchronization bits zero to m bits. In order to determine the location of A1 bits in the header the bits must be selected by the DATA SCANNER. The frame aligner eventually determines A2 byte and thus after determining the location of the sync bits determines the location of the frame per col. 1 line 5-col. 9 line 47.)

It would have been obvious to add the frame aligner or decoder reading the first arrangement of synchronization bits to organize the first stream of information into a first frame structure including a data section and a header section, having a plurality of M bits, the decoder having a second input for selecting the first arrangement of synchronization bits to be read by selecting a number of synchronization bits in the range from zero to m bits, selecting the bit position of the synchronization bits in the header section, and selecting the content of each synchronization bit in the header section of Ikemura which performs STS-N or SONET processing to the decoder of Ishimatsu in order to perform SONET frame processing.

In Addition Ikemura teaches:

Regarding **Claim 23**, a deinterleaver circuit having an input to receive the first stream of information, the deinterleaver circuit deinterleaving the first stream into a plurality of N parallel data streams (The secondary reference teaches that the STM can be made into Z –bit wide units of parallel data per col. 9 line 33-47. It would have been obvious to one of ordinary skill in the art at the time of the invention that breaking he STM can be made into Z –bit wide units of parallel data performs the same function as the interleaver circuit)

In which the decoder's first input includes a plurality of n inputs connected to the deinterleaver to receive the first stream of information in parallel data, the decoder's selecting of the first arrangement of synchronization bits includes selecting an arrangement of synchronization bits in each of the n parallel data streams to form a first frame structure including header and data sections in each data stream (The secondary reference teaches the frame aligner of Figure 2 and then explains that the STM can be made into Z –bit wide units of parallel data per col. 9 line 33-47. It would have been obvious to one of ordinary skill in the art at the time of the invention that breaking the STS-N into different Z-bit wide parallel units performs the same function as the deinterleaver.)

Regarding **Claim 24**, in which the decoder's selection of the first arrangement of overhead bits includes selecting independent arrangements of synchronization bit for each header section of the n parallel data streams (The secondary reference teaches putting A1 and A2 or sync bits into each of the Z-bit wide parallel units per col. 9 lines 34-67. It would have been obvious to one of ordinary skill in the art at the time of the invention that putting A1 and A2 or sync bits into each of the Z-bit wide parallel units performs the same function as arranging the overhead bits including sync bits into n parallel data streams.)

Regarding **Claim 25**, in which in which the deinterleaver circuit detinterleaves the first stream of information into four parallel data streams; and in which the decoders first arrangement of synchronization bits includes reading a first group of bits from the first parallel data stream section, reading a second group of bits from the second parallel data stream header section, reading a third group of bits from the third parallel data stream section, and reading a fourth group of bits from the fourth parallel data stream header section (The secondary reference teaches putting A1 and A2 or sync bits into each of the Z-bit wide parallel units for N STMs per col. 9 lines 34-67. It would have been obvious to one of ordinary skill in the art at the time of the invention putting A1 & A2 into N Z bit wide parallel units could also be performed for four groups)

Regarding **Claim 26**, further comprising: an encoder having an output to provide a second stream of information organized in the first frame structure with header sections, the encoder having an input of selecting a second arrangement of synchronization bits to be written in the header section (The secondary reference teaches putting A1 and A2 or sync bits into each of the Z-bit wide parallel units per col. 9 lines 34-67. It would have been obvious to one of ordinary skill in the art at the time of the invention putting A1 and A2 or sync bits into each of the Z-bit wide parallel units performs the encoder function).

Regarding **Claim 27**, in which the encoder organizes the second stream of information into a plurality of n parallel data streams , and in which the encoder selection of the second arrangement of synchronization bits includes selecting the synchronization bits to be written in the header section of the n parallel data streams, the encoder having a plurality of n output to provide the n data streams (The secondary reference teaches putting A1 and A2 or sync bits into each of the Z-bit wide parallel units per col. 9 lines 34-67. It would have been obvious to one of ordinary skill in the art at the time of the invention putting A1 and A2 or sync bits into each of the Z-bit wide parallel units performs the encoder function. It would have been obvious to one of ordinary skill in the art at the time of the invention that the process be repeated for a second stream) and further comprising:

An interleaver circuit having a plurality of n inputs connected to n encoder outputs, the interleaver circuit interleaving the parallel data streams in to the second stream of information, the interleaver circuit having an output connected to the repeater output (The secondary reference teaches breaking the STM-N into N parallel streams of z-bits per col. 1 line 5 –col. 9 line 47. It would have been obvious to one of ordinary skill in the art at the time of the invention

to perform the inverse function or recombine the parallel streams into a serial stream prior to transmission

In Addition Ishimatsu teaches

Regarding **Claim 28**, in which the repeater input receives the first stream of information in a protocol selected from the group consisting of datacom, telecom, fibre channel, SONET, SDH, and Gigabit Ethernet protocols (SONET per Abstract)

Referring to **Claim 29**, Ishimatsu (U.S. Patent No.: 6,018,406) teaches: A selectable frame synchronization structure communication system (Fig 2 & Fig 3)

A transmitter having an output to provide a first steam of information in a first frame structure with a header including a first arrangement of synchronization bits of the first stream of information (300 & 400 per Fig 3 or transmitter. Please note that it would have been obvious to one of ordinary skill in the art at the time of the invention to integrate the functions of 300 & 400 per Fig 3 into a single unit in order to save space)

A repeater input port to accept a first stream of information including a first arrangement of synchronization bits (600-1, 600-2,...600-m per Fig 3. Please note that it would have been obvious to one of ordinary skill in the art at the time of the invention to integrate the functions of 100 and 200 per Fig 3 into a single unit in order to save space)

Decoder having a first input connected to the repeater input port to receiving the first stream of information (126 per Fig 2. Please note that it would have been obvious to one of ordinary skill in the art at the time of the invention to integrate the functions of 100 and 200 per Fig 3 into a single unit in order to save space)

And a repeater output connected to the decoder (Decoder per Fig 2)

Ishimatsu does not expressly call for: the decoder reading the first arrangement of synchronization bits to organize the first stream of information into a first frame structure including a data section and a header section, the decoder having a second input for selecting the first arrangement of synchronization bits to be read or

An encoder having an output to provide a second stream of information organized in the first frame structure with a header section, the encoder having an input for selecting a second arrangement of synchronization bits to be written in the header section but teaches decoding per Figs 2 & 3.

Ikemura (U.S. Patent No.; 5,400,369) teaches: the decoder reading the first arrangement of synchronization bits to organize the first stream of information into a first frame structure including a data section and a header section, the decoder having a second input for selecting the

first arrangement of synchronization bits to be read (The secondary reference teaches a frame aligner or decoder which determines the sync bits and organizes the data into frames col. 1 line 5-col. 9 line 47.

An encoder having an output to provide a second stream of information organized in the first frame structure with a header section, the encoder having an input for selecting a second arrangement of synchronization bits to be written in the header section (The secondary reference teaches taking the frames and converting them from serial to parallel by removing the A1, A2, and the payload from the serial data and organizing them into parallel data in which parallel frame has A1, A2, and the payload per col. 1 line 5 –col. 9 line 47)

It would have been obvious to add the decoder and encoder processing of Ishimatsu to the decoder and encoder of Ishimatsu in order to perform SONET frame processing.

In Addition Ikemura teaches:

Regarding Claim 31, further comprising: a receiver having an input connected to the repeater output to accept the second stream of information, the receiver reading the second arrangement of synchronization bits to organize the second stream of information into the first frame structure (The reference previously taught breaking the data into parallel streams per col. 1 line 5- col. 9 line 47. It would have been obvious to one of ordinary skill in the art at the time of the invention that a receiver be present to receive the parallel transmitted words in order for the invention to work).

Claim Rejections - 35 USC § 112

4.0 The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 19 & 23-28 are rejected because the metes and bounds of the claims cannot be assessed.

Referring to Claim 19, What is meant by "selecting a number of synchronization bits in the range from zero to m bits"? How can one select zero bits? The specification teaches that the maximum header size is m bits, does the applicant mean selecting a whole header? Can the value of m be less than the maximum header size?

Referring to Claim 23, What is meant by the deinterleaver circuit. How can de-interleaving be performed when interleaving has not already been performed?

Response to Argument

5.0 Applicant's arguments with respect to **Claims 19, 23-29, & 31** have been considered but are moot in view of the new ground(s) of rejection.

The new reference Ikemrua discloses a frame aligner which is utilized for STS-N processing; therefore, it would have been obvious for one of ordinary skill in the art to utilize the frame aligner functions as encoder and decoder functions in a SONET Repeater because the frame aligner is utilized to perform SONET processing.

It would have been obvious to one of ordinary skill in the art that the frame aligner or decoder per Fig 2 is trying to find the A1 byte and A2 byte in the STM-N frame per Fig 1 so that it can determine the frame structure of the STM frame shown in Fig 1 and the decoder has a DATA SCANNER per Fig 2 searches for the value of A1 shown in Figure 1 by selecting bits 1 to 8, 2 to 9 and so on or selecting the first arrangement of synchronization bits zero to m bits and in order to determine the location of A1 bits in the header the bits must be selected by the DATA SCANNER and the frame aligner eventually determines A2 byte and thus after determining the location of the sync bits determines the location of the frame per col. 1 line 5-col. 9 line 47 or performs the same function as a decoder reading the first arrangement of synchronization bits to organize the first stream of information into a first frame structure including a data section and a header section, having a plurality of M bits, the decoder having a second input for selecting the first arrangement of synchronization bits to be read by selecting a number of synchronization bits in the range from zero to m bits, selecting the bit position of the synchronization bits in the header section, and selecting the content of each synchronization bit in the header section.

Please refer to the above rejection for more details.

Conclusion

5.0 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert W Wilson whose telephone number is 571/272-3075. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on 571/272-3078. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert W. Wilson

Robert W Wilson
Examiner
Art Unit 2661

RWW
November 3, 2004

KENNETH VANDERPUYE
PRIMARY EXAMINER